*1.3 Kirchhoff’s Laws and Nodal Analysis*

The analysis of circuits is based *on Kirchhoff’s current law (KCL) and voltage law (KVL). The KCL states that the sum of all currents leaving any node at any time is zero*. This is because charges ideally cannot accumulate at node. (In a real circuit, parasitic capacitances are present at all nodes. Their currents must be included to make this statement valid.) *The KVL states that* *the sum of all branch voltages in a loop is zero.* The Kirchhoff’s laws are illustrated for a simple circuit in **Fig. 1.7.**

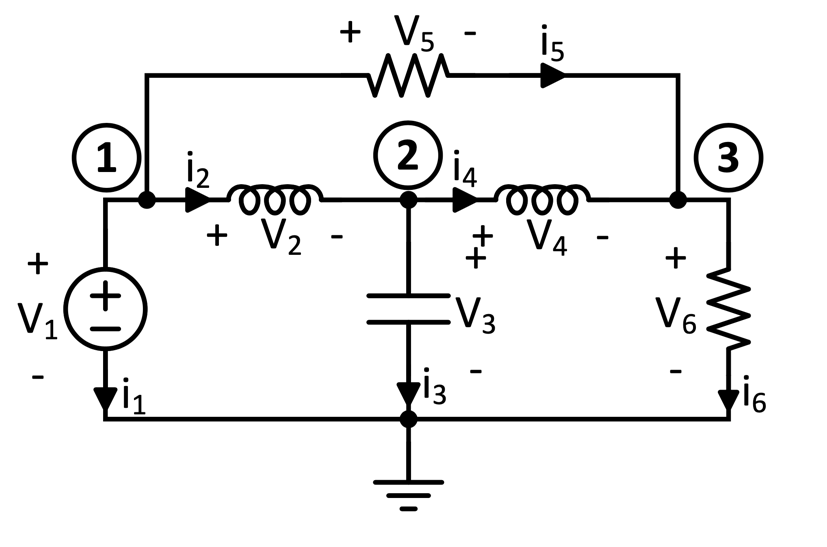


Figure 1.7: Circuit analysis example.

Denoting the current in branch *k* by *ik,* the KCL leads to the relations

Denoting the branch voltages by *vk* and the node voltages by *ei* , the KVL gives the equations

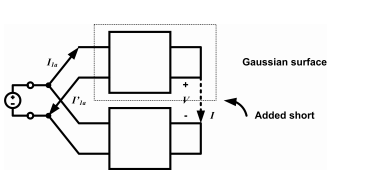
It is efficient at this point to introduce vector and matrix notations. We define the *incidence matrix* ***A.*** Its element in row *I* and column *j* is

The branch currents can be collected into a column vector . Here, *b* is the number of branches in the circuit.Then, the KCLs can be written in the simple form

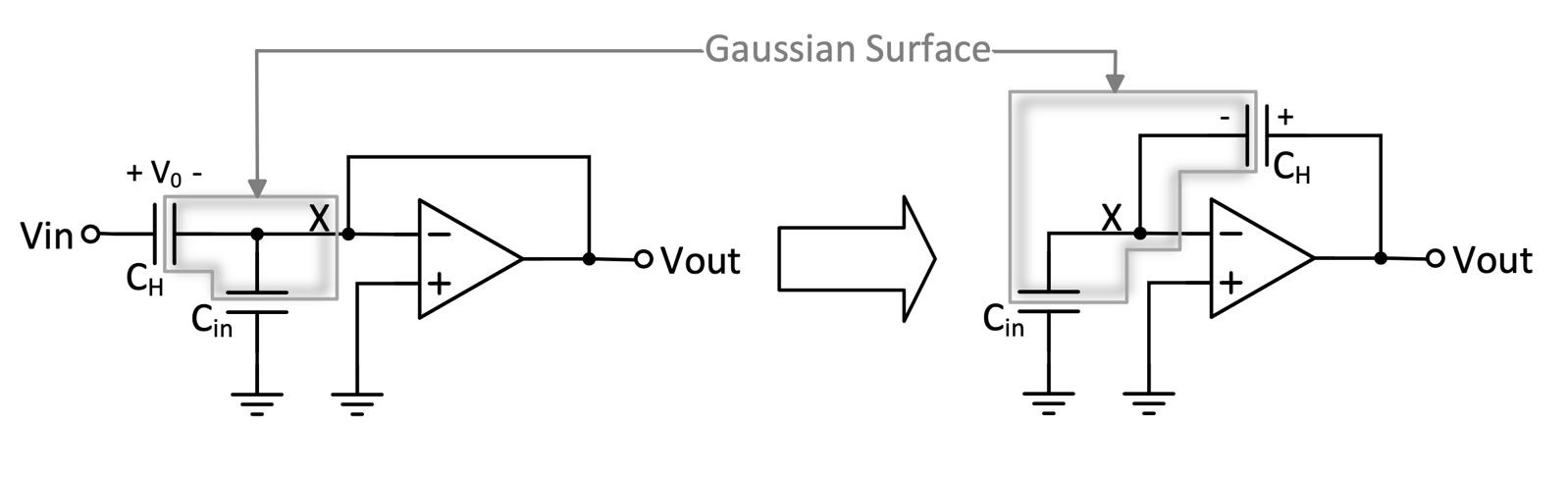
Here, **0**is the column vector of zeros.

Similarly, collecting the branch and node voltages into column vectors, the KVL can be written in the concise form

Kirchhoff’s current law can be generalized. Let a part of the circuit enclosed in a closed surface, sometimes called a *Gaussian surface* (Fig.1.8). Within the surface lie *N* nodes. Since the KCL holds for all these, the sum of all currents leaving them is ∑*i* = 0. Some of these currents flow to nodes which are outside the surface. The branches carrying these connect the circuit inside the surface to the rest of the circuit, and cutting these branches open will cause the circuit to be cut into parts. They are related to the *cutsets* of graph theory. In Fig. 1.8(a), a surface enclosing *C2* and *R3* shows that the currents through these elements are equal. Fig. 1.8(a) shows a test for parallel-connected two-ports. The Gaussian surface proves that in the test circuit both stages function as two-ports before the short is added between their outputs. In Fig. 1.8(b), a surface enclosing *C2* and *R3* shows that the currents through these elements are equal, and hence the charge in the enclosed space remains unchanged.



(a)



(b)

Figure 1.8: Circuits with Gaussian surfaces.

To prove that the total of the currents leaving a Gaussian circuit is zero, note that when we add up the currents leaving the nodes within the surface, those between internal nodes cancel since they leave one internal node but enter another. Thus, the total equals the sum of currents leaving the surface, which therefore also equals zero.

In conclusion*, the sum of currents leaving the part of a circuit within a closed surface is zero.* This is a useful generalization of the KCL. It can be applied in the analysis of both active and passive circuits. Note that the ground and bias nodes are not allowed to be within the surface.

Kirchhoff’s laws are based solely on the configuration (topology) of the circuit. Adding the relationships between branch voltages and branch currents, the circuit can be fully analyzed. Operating in the Laplace transform domain, let *Yii* denote the sum of all admittances connected to node *i*, and let *Yij* denote the sum of all admittances connected between nodes *i* and *j.* We can construct the *nodal admittance matrix* ***Y*** from these admittance parameters such that *yij* is the element in row *i* andcolumn *j*. Then the relation

describes all KCLs for every node. Here, ***I*** is the column vector of the source currents entering the nodes.

Solving (1.12) for the node voltages *ei,* and finding the branch relations from the KVL, the network can be fully analyzed. This *nodal analysis* is the basis of most computer-based circuit analysis programs.

The process is simplified if there are grounded voltage sources in the circuit, since the voltages at their floating nodes are then known. Ungrounded voltage sources, however, require a somewhat more involved process, called *modified nodal analysis (MNA)*. In MNA, in addition to the node voltages in ***e,*** the unknowns include the currents flowing through the floating voltage sources. Consider a circuit with *n* nodes and *s* floating voltage sources. Then we can write *n* KCLs for the nodes, and *s* KVLs for the voltage sources. Thus, for a voltage source *vs1* connected between nodes *a* and *b,* a KVL of the form is added to the set of equation. The equations can then be solved for the *n* node voltages and *s* currents through the voltage sources. Combined with the branch relations, this allows the complete analysis of the circuit.

Fig.1.9 shows an example of a circuit containing only resistors and current sources, which can be analyzed using nodal analysis.

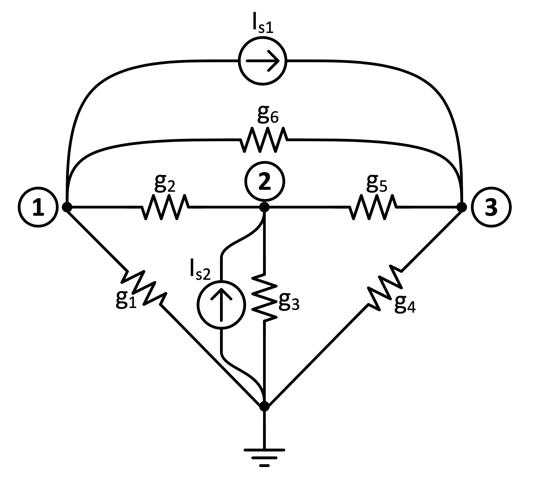


Figure 1.9. Circuit containing conductances and current sources.

The nodal equations are shown below. They are of the form ***G.v = Is***, where ***G*** is the conductance matrix, ***v*** is the vector of node voltages, and ***Is*** is the source vector.

Figure 1.10 shows a similar circuit containing two floating voltage sources. Hence, direct nodal analysis cannot be used. Using the modified nodal analysis, the augmented nodal equations (1.14) result, which need to be solved for the node voltages and the currents *is1* and *is3* flowingthrough the voltage sources.

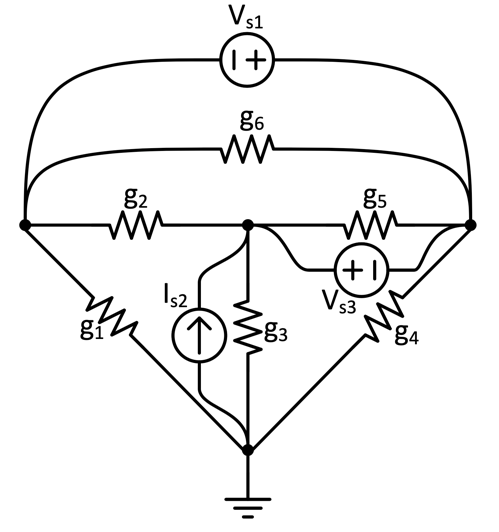


Figure 1.10. Circuit with two floating voltage sources.

***G***

Sometimes, a floating voltage source has an impedance in series. Then, it can be transformed into a floating current source using Norton’s equivalent circuit **(Fig. 1.11)**. This allows using simple node analysis of the circuit.

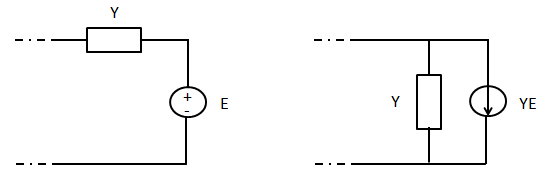
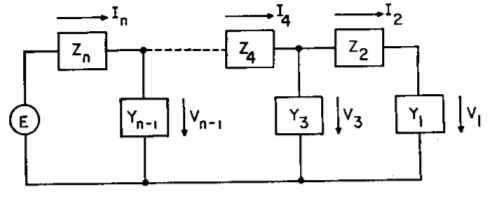


Figure 1.11: Norton’s equivalence

*Example:* **Fig.1.12** shows a *ladder* network, built from an alternation of series and shunt branches. Such circuits are used extensively in passive filters. They also play an important role in the design of analog-to-digital and digital-to-analog data converters, as well as in the modeling of interconnects on an integrated circuit or printed circuit board. We assume that the circuit is linear and time-invariant.



Redraw with currents shown in wires and voltages with +/-.

Figure 1.12: Ladder network.

By applying KVL and KCL alternatively starting with the input branch and working forwards, the equations

result. This is a set of *n* linear equations in the *n* unknowns . The coefficient matrix has a special *tridiagonal* form, which allows a simple iterative algorithm for finding all unknowns [T.R. Bashkow, IRE Trans on Circuit Theory, June 1961]. From these, the remaining variables can be found from the branch relations. The solution process has a simple physical interpretation. Assume that the *output* voltage *V1* is known, and is equal to 1 volt, and that we need to find the *input* voltage *E1* for this output voltage. Then, starting with the output branch, and working *backwards*, we can find all unknowns one at a time. Thus, *I2*. Next, we find *.* Then, , etc*. …,* until *Vn-1* and finally *In* are found. Then, the “unknown” input source is given by . At this point, we know the transfer function . Since the circuit is linear, all actual voltages and currents can be obtained by multiplying the calculated values by .

An important example of a ladder network is the *R-2R ladder,* shown in Fig. 1.13. Analysis using Bashkow’s method gives *V1* = 1 *, V3 =* 2*, V5*  = 4*,* … Thus, the node voltages and the currents flowing in the 2*R* resistors are both binary weighted. This property of the circuit makes it a useful stage in digital-to-analog converters (DACs) [*Carusone book].* Note that an even simpler way to analyze the *R-*2*R* ladder is to realize that the resistance seen to the *right* of each floating node is2*R,* while that seen to the *left* of the node is *R.* Thus, the circuit acts as a cascade of voltage and current dividers, scaling all quantities by powers of 2.

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Figure 1.13: The R-2R ladder.